REMARKS

Claims 1, 7, 13, 18, and 22 are amended. Claims 1-26 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

Claims 1-26 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Onishi et al. (5,383,151), Juengling et al. (5,756,390) and Fazan et al. (IEDM 92). Claims 7-26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Onishi et al., Juengling et al. and Fazan et al. and further in view of Aoki et al. (5,747,844).

The Examiner alleges that the title is not descriptive and requests a new title (page 2 of paper no. 6). The preamble of claims 1-12 recite "memory integrated circuitry" which is verbatim the title language. The preamble of claims 13-26 recite "dynamic random access memory circuitry" which is memory integrated circuitry as recited in the title. Accordingly, the title is descriptive and Applicant respectfully requests withdrawal of the new title request in the next office action.

Claims 1-26 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite because claims 1, 7, 13, 18, and 22 recite "equal to less than." Applicant has amended the respective claims to recite "equal to **or** less than",

and therefore, such claims are definite. Applicant respectfully requests withdrawal of the §112, second paragraph rejection in the next office action.

Claims 1-6 stand rejected under §103 over the combination of Onishi, Juengling and Fazan. Claims 7-26 stand rejected under §103 as being unpatentable over the combination of Onishi, Juengling, Fazen, and Aoki. That is, both rejections rely on Juengling. However, the use of Juengling as prior art is improper under Section 35 U.S.C. §103(c). Accordingly, the obviousness rejections are inappropriate and must be withdrawn.

Juengling, U.S. Patent No. 5,756,390, and the above-referenced application, are commonly owned. MPEP §706.02(l)(3) states that such commonly owned reference is disqualified when:

> (a) proper evidence is filed [referring to the statement of common ownership];
> (b) the reference qualifies under 35 U.S.C. §102(e) for applications filed on or after November 29, 1999; and
> (c) the reference is used in an obviousness rejection under 35 U.S.C. §103(a).

A separate statement establishing common ownership is filed herewith. The Juengling reference qualifies as a §102(e) reference and is used in the obviousness rejections against claims 1-26. Moreover, the above-referenced application was filed after the November 29, 1999 deadline. Accordingly, the requirements of MPEP §706.02(l)(3), and therefore §103(c), are met. Consequently, the obviousness rejections against claims 1-26 based on Juengling are inappropriate and must be withdrawn. Applicant respectfully requests withdrawal of such rejections in the next office action.

Since no other rejections are presented against claim 1-26, such claims are allowable. Applicant respectfully requests allowance of such claims in the next office action.

Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed together with this application on August 14, 2001. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 2-13-03

By: _____

D. Brent Kenady
Reg. No. 40,045

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/930,787
Filing Date . . . . . August 14, 2001
Inventor . . . . . Luan Tran
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2814
Examiner . . . . . Howard Weiss
Attorney's Docket No. MI22-1784
Title: Memory Integrated Circuitry

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO NOVEMBER 13, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (Amended) Memory integrated circuitry comprising:

an array of memory cells formed in lines over a semiconductive substrate and occupying area thereover, the respective area consumed by at least some individual memory cells within the array being equal to or less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

7. (Amended) Memory integrated circuitry comprising:

an array of memory cells formed over a semiconductive substrate and occupying area thereover, at least some memory cells of the array being formed in lines of active area formed within the semiconductive substrate which are continuous between adjacent memory cells, said adjacent memory cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent memory cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

13. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

18. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a bulk silicon semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, the word lines and bit lines having respective conductive widths which are less than or equal to 0.25 micron, the DRAM cells within the array being formed in lines of active area formed within the silicon substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by respective conductive lines formed over said continuous active area between said adjacent DRAM cells;

at least some adjacent lines of continuous active area within the array being isolated from one another by LOCOS field oxide formed therebetween, said LOCOS field oxide having a thickness of no greater than 2500 Angstroms;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than 0.5 micron^2; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

22. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than $8F^2$, where "F" is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

END OF DOCUMENT

EL844046303

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/842,230
Priority Filing Date ..... April 22, 1997
Inventor ..... Luan Tran et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2814
Priority Examiner ..... H. Weiss
Attorney's Docket No. MI22-1784
Title: Memory Integrated Circuitry

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 08/842,230, filed April 22, 1997, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). As a courtesy, Applicant submits copies of the cited references for review.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: Aug 11, 2003

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138